



09/874894

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	William Jones et al.	Examiner:	Thong Le
Serial No.:	09/874894	Group Art Unit:	2818
Filed:	June 5, 2001	Docket No.:	303.764US1
Title:	CONTROLLER FOR DELAY LOCKED LOOP CIRCUITS		

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RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

REMARKS

This is in response to the Office Action mailed on January 29, 2004.

No claims are amended. Claims 1-29 and 42-53 are now pending in this application.

*Reservation of the Right to Swear Behind References*

Applicant maintains the right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

*§102 Rejection of the Claims*

**Claims 1-29 and 42-53 were rejected under 35 USC § 102(b) as being anticipated by Kobayashi et al. (U.S. Patent No. 5,675,274).**

Applicant respectfully traverses.

Kobayashi et al. discloses in FIG. 1 a DLL (2) for generating an internal clock signal (C") based on either a reference clock signal (C) or a test clock signal (Ctest). A selector (1) of Kobayashi et al. selects the reference clock signal C to generate the internal clock signal C" during a normal operation. Selector 1 selects the test clock signal Ctest to generate the internal lock signal C" during a test. As shown in FIG. 1 of Kobayashi, regardless of which of the reference clock signal C and the test clock signal Ctest is selected to generate the internal clock signal C", the DLL of Kobayashi et al. performs a synchronization operation to synchronize the internal clock signal C" and the reference clock signal C.